Department of Computer Science
Duke University
Ph.D. Qualifying Exam

Computer Architecture
2:00 pm-5:00 pm August 21, 2014

Instructions

• Answer all questions: some questions may have several parts.
• Write your code number on each page of this exam.
• Be sure to provide code sequences and/or examples to support answers when requested.
• State all of your assumptions explicitly.
• Show all of your work.
• You have three (3) hours to complete this exam.
• This is a closed book/notes exam.

Policy on Misprints and Ambiguities
We have made every effort to carefully proofread this exam, and make the questions clear and concise. If you believe a problem is stated incorrectly, notify the proctor immediately. In any event, include your interpretation of the problem in your written answer.

Good Luck!
Question 1. Performance

a) [10 pts] Processor P has a 1ns clock cycle time with CPIs of: LD 3, ST 1, FADD 1, FMUL 3, FDIV 12. Given a program that executes 10 Million instructions with the instruction composition of LD 33%, ST 17%, FADD 25%, FMUL 15%, FDIV 10%, compute the execution time on processor P. Show your work.

b) [10 pts] An optimization reduces the time for task A by a factor of 10. Compute the speedup achieved by this optimization for two programs P1 and P2. Task A is 20% of P1 and it is 60% of P2. Show your work.
Question 2. Pipelining

a) [10 pts] Explain how pipelining can improve performance of a processor. Provide a code sequence as an example to support your explanation.

b) [10 pts] List and explain three reasons that the performance improvement achieved by pipelining may be not reach the maximum theoretically possible.
Question 3. Processor Design

a) [15 pts] Explain why register renaming is important and describe one way to implement renaming. Use a code sequence to demonstrate your implementation and show how it improves performance compared to a processor without register renaming.

b) [5 pts] What is the relative benefit in power reduction of decreasing a processors clock frequency from 3 GHz to 1.5 GHz compared to decreasing the voltage from 1.2 V to 1.0 V?
Question 4. Cache Memory Hierarchies

a) [5 pts] Write down the average memory access time equation for a three level cache hierarchy.

b) [15 pts] Assume a system has 64-bit virtual addresses, 36-bit physical addresses, and 4 KB virtual memory pages. Draw a block diagram of the following memory system. A 128 entry direct-mapped TLB, a 64 KB 2-way set-associative physically indexed, physically tagged, write-back cache, with 64 Byte blocks.
   Clearly indicate how many bits are used for the index and tag of each structure, and how the appropriate data is selected assuming full word (64-bit) load/store instructions. Also clearly show where the TLB is placed with respect to the cache.
Question 5. Miscellaneous Topics

a) [5 pts] Briefly explain the difference between a VLIW processor and a superscalar processor.

b) [8 pts] Describe the advantages and disadvantages of bus-based snooping coherence vs. directory-based coherence.

c) [7 pts] How do modern GPUs tolerate long memory latencies? Provide an example to support your answer.