

The Ray-Casting Engine Version 1.5
(VME version)
System Specifications

1.0 Introduction

This document describes the Ray-Casting Engine version 1.5. (RCE-1.5) The document describes in details all the system components, the interface to a general purpose machine and the RCE architecture that is visible to the system programmer. This document is addressed to the systems programmer who is going to write device drivers for the RCE and low level interfaces and applications for the RCE. It is also addressed to the hardware maintenance engineer.

This document is constructed as a working document by the RCE development group and is subject to continual changes. It is assumed that the reader is familiar with the Primitive Classifier (PC) and the Classification Combiner (CC) ICs described in [REF###].

The RCE-1.5 is an upgrade to the third generation Ray-Casting Engine (RCE-1.0). The current implementation uses the same CC and PC processors uses in RCE-1.0 but upgrades the system interface and recirculation hardware.

The RCE1.0 is a special purpose computer imbedded inside the ADAG-3000 frame buffer. The RCE1.5 is designed to overcome and remove some of the deficiencies of the RCE1.0.

The biggest computational bottle-neck in the RCE-1.0 is the slow communication between the RCE and it host computer. RCE1.0 uses the Q-bus connection of the ADAG-3000 as the only means of communication between the host and the RCE. The communication channel is slow and limit the type of computer that can be used as a RCE driver.

The current implementation (RCE1.5) uses the VME as the system bus for the RCE. This decision solves several problems:

- a) The VME bus could provide 4-8 Mbyte/Sec. communication band-width, more than an order of magnitude improvement over the 200K Mbyte/Sec. of the RCE1.0.
- b) The VME standard allow us to buy off the shelf enclosures and power supplies providing mechanical and electrical environment for the RCE.
- c) Using commercial bus adaptors, we can connect the machine to a variety of different families of processors (SUN, DEC, IBM, HP, SGI etc).
- d) Using the extra slots on the VME bus one could add options to the RCE such as frame buffer or compute engine.

The RCE is a special purpose computer dedicated to a single computation, namely: ray-casting of solids represented by Constructive Solid Geometry (CSG solids). The heart of the machine is a $(\text{Log}(N)+1) \times N$ array of custom, bit-serial processors: CCs and PCs, dedicated to raycasting. The reader should refer to [REF####] in order to learn about the theory and implementation of the CC and PC custom processors.

The RCE-1.5 system can accommodate up to eight boards with PCs and CCs. The boards are called extension boards. Each extension board holds up to 16-PC chips and 4x16 array of CC chips. Each PC chip holds four PC processors and each CC chip hold a 2x4 array of CCs for a total of 64 PCs and 512 CCs per board. A standard configuration of the machine has four extension boards with 256 PCs and 2048 CCs.

In addition to the Extension boards the RCE has three other major components: The base board, the dual port memory card, and VME to host-bus adaptor. The base board houses all the major control and interface functions for the RCE. The DMA memory card is a commercial dual port memory buffer. One port is on the VME bus, allowing the host to read and write into the buffer and thus transfer large ray files in and out of the RCE. The other port is on a privet VSB bus connecting the memory buffer to the base card.

The RCE 1.5 system solves the data storage and communications problems that RCE 1.0 has. The RCE 1.0 system was designed as a demonstration system. No special attention was paid to balancing computation speed with I/O bandwidth and storage requirements. The main goal in building RCE 1.0 was to prove that a scalable architecture could be built and that the core of the system is capable of Ray-Casting complex CSG objects at high speed. While RCE 1.0 did meet these goals, as a system it has some major deficiencies. Since no follow-up system is planned we have decided to keep the core array of processors (PCs and CCs) and address the major system level deficiencies. RCE 1.0 system has three major bottlenecks:

- a. Slow communication between the host and the RCE.
- b. Limited local memory buffer for recirculation.
- c. Slow data access for recirculation.

The RCE 1.5 system was designed to address these deficiencies and to add functionality to the system where it could be done at low cost with a large payoff (by reducing the host post processing requirements). RCE 1.5 has the following enhancements:

1. Large internal memory buffer (96 Megabytes) for storing intermediate files.
2. Dual bus system in the PC/CC array for simultaneous recirculation of data.
3. Dedicated hardware for data recirculation with data decompression.
4. On line data compression (not implemented yet)
5. (standard) VME bus interface.
6. Dual port memory buffer for host to RCE communication.
7. On-line front surface gradient calculations for shaded object graphics. (not implemented yet).
8. On-line Small segments and gaps filtering, cross section area calculations and bounding box calculations (not implemented yet).

The RCE 1.5 system is made of the following physical components: A 12 slot VME tower enclosure, a triple height double width (9U) VME card base that implements most of the system interface functions, a set of one up to eight of 9U VME cards that holds the PC/CC array, a single 6U dual port 4-8 MegB memory card with a VME-VSB interface. A single slot VME to host-bus interface card. In addition there is a single empty VME slot that can be used to house a pre/post raycasting processor.

The base card is the main controller for the RCE. Figure 1 shows a block diagram of the system. Figure 2 describes the major components on the base board. The base board provides several functions that enhance the functionality and performance of the RCE. It holds the following subsystems:

- a) VME bus interface unit.
- b) The Local Bus.
- c) Two recirculation subsystems (Units A and B).
- d) The RCE DMA interface and shading unit
- e) The recirculation memory buffer.
- f) DMA interface to the VSB bus.

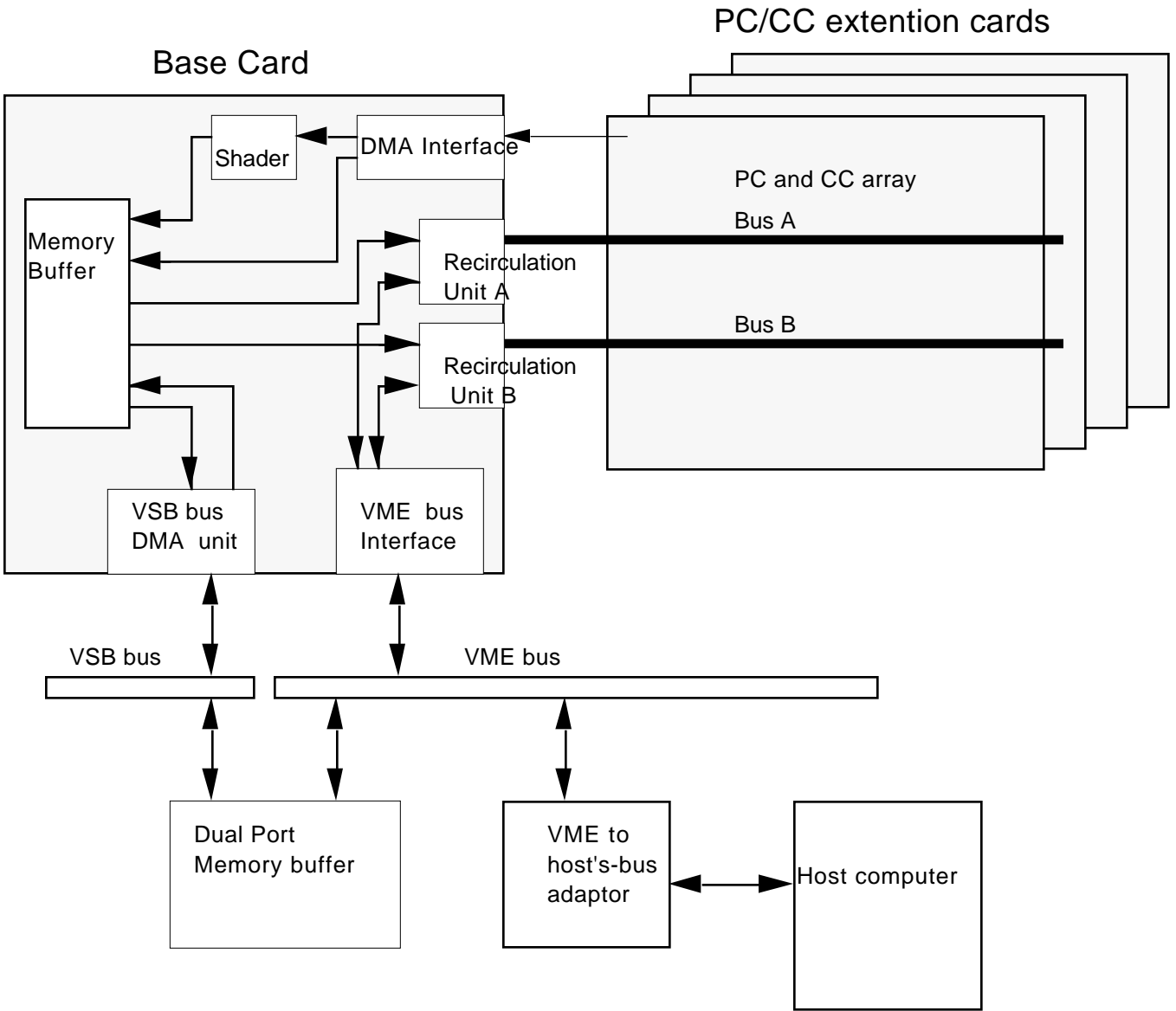


Figure 1: RCE-1.5 Block Diagram

The VME interface unit connects the base board to the VME bus. The unit translates the VME addresses to RCE internal addresses and transfers interrupts and register values between the RCE and the VME master. The base board is a VME slave board. All direct communication between the host and the RCE is done through reading and writing registers. The host controls the RCE operation by writing values into registers. The RCE notify the host when the operations are done through an interrupt line. The host then read a sequence of status registers to find out what happened. All reads a writes of internal RCE registers are done by the host trough the VME. With the exception of recirculation data that is fed by the recirculation unit. The VME interface unit translates the VME addresses into the local bus addresses or to the A-bus and B-bus addresses that connect to the PCs in the extension cards.

The local Bus is the internal connecting tissue for the RCE. The local bus connect all internal command and status registers on the base board to the VME bus. The local bus is used for control only. All the units on the bus act as slaves. only the VME interface unit acts as a master, allowing the host to read and write all the internal registers.

The recirculation subsystem reads large compressed ray files residing in the recirculating memory buffer, decompresses the ray files and loads the files into the ray-casting array through one or two PCs. The recirculation unit has two recirculation subunits unit-A and unit-B. Each unit is connected to a bus (Bus-A or Bus-B) that connects to half of all the PCs in the array. All the even numbered PC chips are connected to bus A and all the odd ones to bus B. The units work independently and can load simultaneously two ray files into the RCE array. Each recirculating unit can be programmed to connect to a single PC on its bus, monitor the PC status, and load a packet of data from the ray file into the PC when it is ready to receive new data.

The RCE DMA interface and shading unit is a unit that process the data stream coming out of the RCE array, it filters the ray file data, compresses the ray file data, computes gradient information as well as other useful values such as cross section area, bounding boxes, etc. The DMA interface unit is implemented as a single IC with an external FIFO that delay the ray file data by a single scan line for gradient calculations. The unit transfer the ray file data into

The recirculation memory buffer is a large (32 Mega-words) memory buffer designed to hold ray files that are part of incomplete computation or the result of ray-casting calculation. The buffer is designed to hold many ray files at the same time simplifying the implementation of time sharing on the RCE. The memory buffer implements a six port memory through six FIFO connections to other units. There are three input FIFOs and three output FIFOs connected to the memory buffer. Two FIFOs, one input, one output, connect the memory buffer to the VSB bus allowing an on-board DMA unit to transfer blocks of data to and from the external dual port memory. Two output FIFOs connect the memory buffer to the recirculation units (unit-A and unit-B). Two input FIFOs receive data streams from the DMA interface and shading unit. One FIFO receive ray file data and the other receive gradient data. Controlling the FIFOs, on the memory buffer side, is a control unit that empties or loads blocks of data from the FIFOs into and out-of the memory buffer. The unit handles all the buffers simultaneously and in addition refreshes the memory buffer. All data transfers between the memory and the FIFOs are done in 512 word blocks. The block transfers are designed to increase the memory transfer bandwidth.

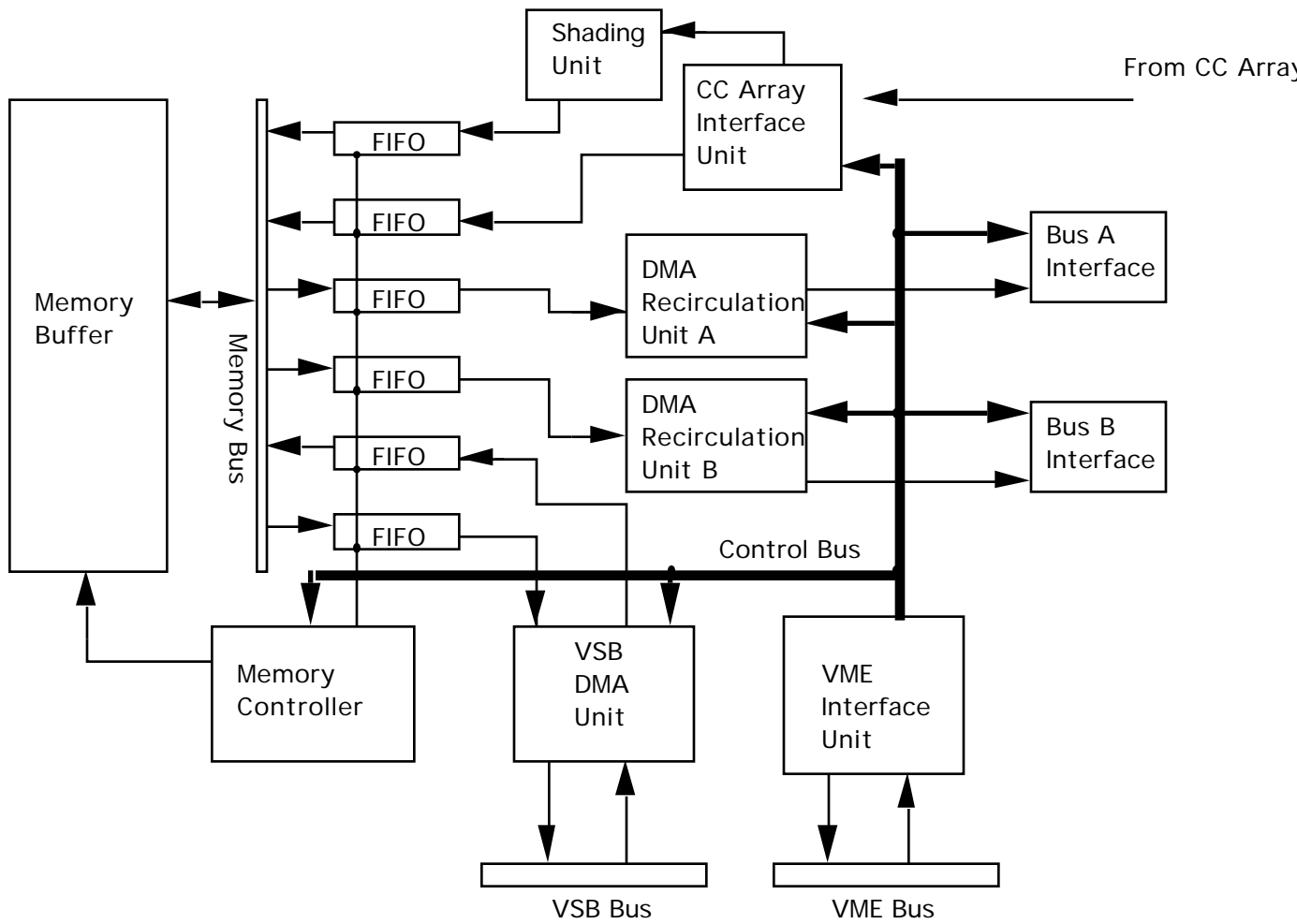


Figure 2: Base-board Units