Exploiting Dark Fluorophore States to Implement Resonance Energy Transfer Pre-Charge Logic

Resonance energy transfer (RET) logic uses self-assembled networks of fluorescent molecules to perform computation at scales far below the diffraction limit and in environments that preclude silicon electronics. In this article, the authors propose a new form of RET logic design, which yields a library of nonlinear logic gates that can be cascaded to build more complex integrated molecular circuits.

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The incredible reduction in feature sizes achievable by lithographic fabrication has led to smaller, faster, and more computationally complex integrated circuits. Yet, even as transistor sizes approach fundamental scaling limits, certain computational domains remain inaccessible to silicon-based integrated circuits. The aqueous environments necessary for biological applications, for example, are generally incompatible with current computational methods, simply due to the materials and operating principles of semiconductor devices. Thus, there is a need for a circuit technology that can introduce computation to these unexplored, molecular-scale domains.

Resonance energy transfer (RET) logic provides a route toward building integrated molecular circuits for such applications.[1] In this technology, networks of fluorescent molecules are spatially arranged with angstrom-level resolution using inexpensive, self-assembled DNA nanostructures. RET-based circuits move and manipulate data in the form of exciton currents, similar to the carrier currents that dictate the functionality of semiconductor devices. The unique composition and molecular scale of these circuits make them compatible with various untapped computational domains.

When introduced to a liquid, for instance, RET circuits can diffuse about, sensing, analyzing, and reporting the liquid's contents back to the user. Using a technique known as *integrated sensing*, analytes such as proteins and RNA fragments can bind to the DNA substrate,

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altering exciton flow within some portion of the circuit and providing a method of on-chip, label-free detection.[2] RET circuits can then directly use this information to perform calculations at the point of detection—for example, counting the number of binding events or determining the analyte's association and dissociation constants.[3] More conventional methods of performing these measurements typically require extensive wet-lab work (for instance, labeling and/or quantitative affinity chromatography), and other forms of molecular-scale computing, such as DNA-based logic gates, can perform similar computation in these same aqueous environments but at much slower speeds.[4] Furthermore, with experimental evidence mounting that DNA nanostructures can be directly fabricated by living organisms, RET circuits may offer a route toward real-time analysis and manipulation of cellular information, for example, by releasing therapeutic cargo with photo-cleavable molecules after performing the embedded sensing and computation.[5,6] These are just a few of the potential applications in which RET logic can perform biologically relevant molecular-scale computation that is likely to remain challenging for traditional silicon-based devices.

Despite the potential benefits, examples of RET logic thus far are predominantly limited to demonstrations of single gates with little attention paid toward building complex circuitry. We address this lack of complexity by introducing a new style of RET logic design called *Pre-Charge Logic*. PCL leverages the dark states of fluorescent molecules, named for their transient lack of fluorescence, to modulate RET networks by temporarily turning certain molecules off. Using this concept, we construct a library of nonlinear RET logic gates including AND, OR, NAND, NOR, XOR, XNOR, PASS, and Negated PASS (NPASS), most of which are unachievable by conventional RET logic. Furthermore, these logic gates can be cascaded with one another to implement complex logic that requires fewer unique fluorophores than previous cascading techniques. To support these design methods, we provide preliminary experimental data for a PASS gate. We also model each gate as a continuous-time Markov chain (CTMC), allowing us to validate general PCL operating principles and explore the design parameters essential to optimizing gate performance. Lastly, we show how to cascade PCL gates to form more complex circuits.

Resonance Energy Transfer Logic

Exploring PCL requires a basic understanding of fluorescence, RET, and the operating principles of existing RET logic.

Fluorescence and Resonance Energy Transfer

RET logic consists of fluorescent molecules, or *fluorophores* (sometimes referred to by the broader term *chromophores*), that absorb and re-emit certain wavelengths of light on the basis of their excitation and fluorescence spectra, respectively. When a fluorophore absorbs a photon, it is elevated to an excited state, which generates a molecular exciton—that is, an electron-hole pair that is bound to the molecule. An excited fluorophore eventually returns to its ground state spontaneously, recombining the electron-hole pair and releasing the remaining energy either as photons (that is, fluorescence) or heat. This spontaneous decay follows an exponential probability density function of the form $e^{-t/\tau}$, in which τ represents the lifetime of the fluorophore's excited state, typically on the order of a few nanoseconds.[7]

When an excited fluorophore is placed 1 to 10 nanometers from a separate, ground-state fluorophore, the excited molecule may donate its exciton non-radiatively to its neighbor through RET. For RET to proceed, the donor's emission spectrum must overlap the acceptor's excitation spectrum. This requirement forces RET to be a predominantly one-way transfer mechanism, much like a standard p-n junction diode. However, transfer can occur between two instances of the same fluorophore in a process known as *homo-RET*, leading to exciton diffusion given the bidirectionality of this process.

RET efficiency heavily depends on the distance between fluorophores. Thus, nanometer-scale control over intermolecular distances is required to properly design RET systems. To achieve this spatial resolution, DNA nanostructures are used as molecular scaffolding for arranging fluorophores.[1–3] DNA sequences are designed such that when mixed together they assemble into a predefined structure

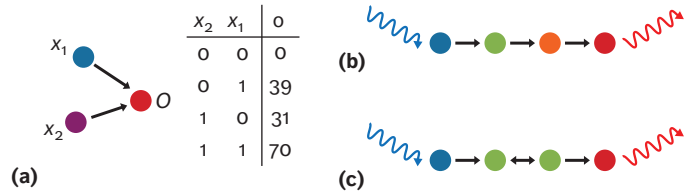

Figure 1. Examples of previously proposed resonance energy transfer (RET) logic components. (a) Exciton flow diagram (EFD) for an OR gate along with the resulting fluorescence recorded from all input conditions. (b) EFD for a hetero-RET wire. (c) EFD for a homo-RET wire.

simply due to the rules of base complementarity (A binds to T and C binds to G). Before assembly, fluorophores are attached to specific locations along the DNA strands, allowing them to be predictably positioned throughout the resulting nanostructure. Trillions of nanostructures, each containing a RET network, can be fabricated in a matter of hours through a few simple pipetting actions (assuming 100 microliters of a final 1 micromolar solution). The overall yield of this assembly process does depend on the target nanostructure, but yields can be as high as approximately 90 percent.[8,9]

RET Logic Components

Using DNA self-assembly, we can arrange fluorescent molecules into networks that perform logic operations similar to those of conventional digital logic. Photons supplied by wave guides or external sources act as inputs to these networks, generating excitons at designated wavelength-multiplexed input fluorophores. These excitons then travel through the network via RET until reaching an output fluorophore, which conveys the result of the computation back to the user through fluorescence. The output fluorescence from an ensemble of devices is monitored by a nearby photodetector. When this signal rises above a predefined threshold, the result is interpreted as a logical 1; otherwise, it is interpreted as a logical 0.

Figure 1a illustrates the exciton flow diagram (EFD) for a RET-based OR gate previously fabricated in our lab.[3] Distinct fluorophores are represented by different colors corresponding to the relative portion of the visible spectrum occupied by that fluorophore. RET paths are depicted as arrows extending from donors to acceptors. The OR gate consists of three molecules: two spectrally distinct input donors, x_1 and x_2, and a single RET acceptor, O, which acts as the gate's output. Exciting either input independently results in RET, and subsequently, output fluorescence. Exciting both inputs simultaneously results in roughly double the output emission. By setting the output threshold below the fluorescence values provided by each independent input, the resulting truth table is equivalent to that of a standard OR gate. This same device can also be reconfigured to an AND gate by simply raising the threshold above the individual contributions such that both inputs must be true to produce a logical 1.

Individual logic gates are connected by chains of donor-acceptor pairs that form excitonic wires. Figure 1b illustrates a hetero-RET wire, which uses a linear cascade of distinct fluorophores to transport excitons. Hetero-RET wires provide unidirectional exciton transfer but quickly consume the visible spectrum available for building RET systems, because the number of required unique fluorophores scales with the wire length. Homo-RET wires, shown in Figure 1c, use multiple copies of the same fluorophore and therefore conserve spectral content with increasing length at the expense of bidirectional transfer. To induce directionality, excitons can be constantly supplied at the input such that the occupancy of upstream fluorophores forces downstream excitons to move toward the output.

A few important limitations of previously proposed RET logic prevent the construction of complex circuits. First, there is no inversion since it is difficult to create the absence of excitons from the presence of excitons using the design concepts described thus far. Furthermore, under standard operating conditions, the outputs of RET logic gates are always linear combinations of their inputs. For example, even when only a single input is supplied to the gate of Figure 1a, the output is still roughly half of the total possible fluorescence. If this device is configured to perform an AND operation, this significant output fluorescence, which should represent a 0, may lead to the incorrect evaluation of downstream logic. To avoid this, logic gates ideally should have tunable nonlinear responses in which the output

from a logical 1 is much greater than the output from a logical 0.

In addition to the lack of inversion and nonlinearity, when cascading gates like the one in Figure 1a, the hetero-RET design style implies that every fluorophore of every gate will consume an additional portion of the visible spectrum. Accordingly, the spectral content of a cascade scales as $(m + n)x$, in which m, n, and x represent the number of inputs, outputs, and logic gates, respectively. This quickly exhausts the visible spectrum.

Pre-Charge Logic

To overcome these limitations, we propose RET-based PCL, which manipulates the dark states of fluorescent molecules to dynamically modulate the flow of excitons in RET networks.[10] We use PCL to construct a library of nonlinear logic gates that can be cascaded to evaluate complex logic, while partially decoupling the length of cascades from their spectral consumption.

Dark States

When excited in the presence of certain chemicals (such as β-mercaptoethylamine [MEA], glutathione, or dithiothreitol), fluorophores may transition from their excited state to a dark state.[11] This transition is a low-probability event, requiring many excitation attempts before occurring. The average number of attempts depends on the fluorophore, but typically ranges from hundreds of excitation cycles to tens of thousands of excitation cycles.[12] Once in the dark state, a fluorophore can neither fluoresce nor accept an exciton.[13] Thus, the dark state offers a mechanism for effectively switching off fluorophores in a RET network.

Similar to the standard excited state, dark fluorophores spontaneously return to their ground state. In contrast to nanosecond-long excited state lifetimes, dark states can persist for fractions of a second to hours depending on the molecular pathways involved and the microenvironment conditions.[10,11] Fortunately, dark fluorophores may also be photonically reset to their ground state by UV excitation or by exciting activator fluorophores positioned nearby.[10,13,14] We can use these mechanisms to perform global and input-specific resets, respectively.

It is important to note that some fluorophores are not susceptible to entering a dark state.[15] Categorizing fluorophores into susceptible and nonsusceptible groups lets us design RET devices composed of both types. Dynamic portions of devices are constructed from susceptible fluorophores that are intentionally modulated to implement Boolean logic. Static portions of devices are constructed from nonsusceptible fluorophores, ensuring that those portions remain fluorescent during device operation.

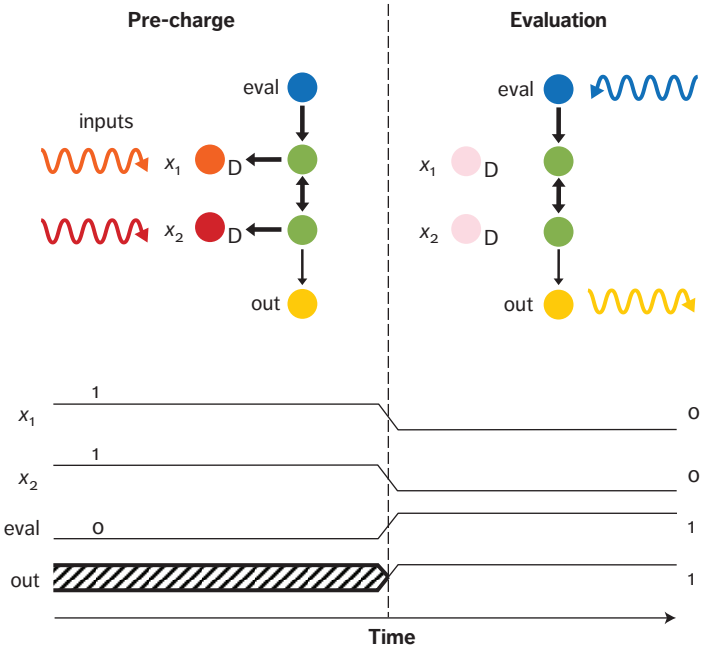

Figure 2. Two-phase operation of the Pre-Charge Logic (PCL) AND gate when both inputs, x_1 and x_2, are true. The time scale may not accurately represent the ratio of the pre-charge and evaluation phase durations. Also, for the sake of simplicity, the time traces shown represent the binary interpretations of the output fluorescence—that is, they are either above or below the 0–1 threshold.

PCL Operation

To demonstrate how the dark state can be exploited to build logic, we use the PCL AND gate depicted at the left side of Figure 2 as an example. This gate is composed of five distinct fluorophores. The "eval" fluorophore acts as the exciton source for the network and is excited to determine the computational result. The "out" fluorophore acts as the gate output. The two fluorophores running through the center of the device are called *mediators*. These molecules form a homo-RET wire connecting eval to out. Lastly, the x_1 and x_2 fluorophores are

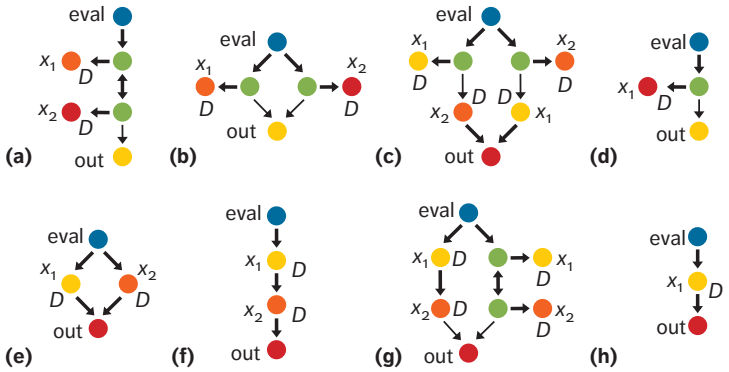

Figure 3. EFDs for (a) AND, (b) OR, (c) XOR, (d) PASS, (e) NAND, (f) NOR, (g) XNOR, and (h) Negated PASS (NPASS) PCL gates. These EFDs include only necessary RET pathways. When implemented with real fluorophores, there may be additional weak, undesirable RET paths between nonadjacent fluorophores.

the inputs to the gate. These fluorophores are annotated with a "D," denoting that they can undergo a dark transition, whereas the rest of the fluorophores cannot. Many PCL gates require a mixture of high and low transfer efficiencies. We illustrate this in EFDs using thicker line weights to denote high transfer efficiencies—for example, for the AND gate, the mediator-to-input transfer efficiencies are higher than the mediator-to-output transfer efficiency.

Inspired by CMOS domino logic, PCL operation is divided into two phases: a pre-charge phase in which the input conditions are established and an evaluation phase in which the output is assessed. During the pre-charge phase, inputs are applied by either an external light source or an upstream RET network that donates excitons to x_1 and/or x_2. If these inputs are true, after many excitation cycles, the input fluorophores transition to their dark states, making them inaccessible as RET acceptors. Note that this transition time may differ for each input since each fluorophore may require a different number of excitation cycles before entering its dark state. For gates with multiple inputs (such as the AND gate), this implies that the pre-charge phase must be long enough to accommodate the input with the slowest transition time. Alternatively, these times can be equalized by adjusting the excitation intensity associated with each input.

Once the inputs are set, the output is assessed by exciting eval with a low-intensity source and monitoring the output. The duration of this evaluation phase should be kept short so as to correctly determine the output before the inputs spontaneously return to ground or are accidentally placed in the dark state by the evaluation process. Determination of the exact pre-charge and evaluation time scales depends on the fluorophores used, as well as a variety of experimental parameters (for example, excitation intensities and reducing agent concentrations). To provide a rough estimate of these time scales, however, we show in the "Experimental Demonstration" section that for a proof-of-concept PASS gate, the pre-charge and evaluation phases are approximately 10 seconds and 5 seconds, respectively.

Figure 2 illustrates the two-phase operation of the PCL AND gate when both inputs are true. During the pre-charge phase, both inputs are excited into their dark states. With these fluorophores temporarily removed, evaluation of the gate results in a high exciton flux from eval to out, and subsequently high output fluorescence interpreted as a logical 1. If either of the inputs is false, the associated input fluorophore would still be available as a RET acceptor. These acceptors would steal excitons from the mediators before reaching the output, resulting in a lower fluorescence signal interpreted as a logical 0. Over time, the device spontaneously resets. To force this reset, a UV source can be applied to the entire structure. Alternatively, exciting wavelength-multiplexed activator fluorophores positioned close to each input (not shown in Figure 2) would allow them to be reset individually.

PCL Gate Library

We can extend the design concepts of the PCL AND gate to create a library of logic gates (see Figure 3).

The OR gate (Figure 3b) achieves its functionality by offering two independent exciton paths from eval to out. Each of these mediators has a corresponding input fluorophore that acts as a RET acceptor. Turning off either input removes that exciton sink, thereby increasing the output fluorescence above the 0–1 threshold. Comparing the OR and AND EFDs,

similarities between PCL and standard switch-based logic design become apparent; devices in series produce AND operations, and devices in parallel produce OR operations.

In addition to these similarities, PCL also adheres to De Morgan's laws, requiring AND and OR to be transposed whenever either operation is inverted. Accordingly, the NAND and NOR gates in Figure 3 are modified versions of the OR and AND gates, respectively. To achieve negation, mediators are directly replaced by their input fluorophores. This allows RET paths from eval to out to be switched off rather than enhanced through the removal of competitive pathways. For example, the NAND gate in Figure 3e has two parallel paths from eval to out, each composed of one input fluorophore. Both inputs must be removed for the output fluorescence to significantly drop.

Close inspection of positive and negative gate pairs, such as AND/NAND and OR/NOR, reveals that positive literals are implemented as mediator-input pairs and negative literals are implemented as inline inputs. Applying these concepts, we constructed the XOR and XNOR gates in Figures 3c and 3g by physically implementing each gate's sum-of-products representation. For instance, XOR comprises the minterms $x_1\overline{x_2}$ and $\overline{x_1}x_2$. The first minterm is constructed by placing an x_1 mediator-input pair in series with an inline x_2 input. Following the same rules, the second minterm is simply the inverse of the first minterm. XOR is then fashioned by summing these two minterms as independent RET paths from eval to out.

During the pre-charge phase, gates using inline inputs can exhibit significant output fluorescence because their inputs are directly wired to the output. The two-phase operation of PCL, however, ensures that this fluorescence does not interfere with an accurate reading of the output during evaluation. There is one additional complexity for NOR and XNOR gates. While pre-charging, excitons may travel downstream and mistakenly turn off other input fluorophores due to their serial layout. If this does occur when implemented with real fluorophores, it can be remedied by applying inputs sequentially starting from the top and resetting all downstream inputs (using additional activator fluorophores) before applying the next input.

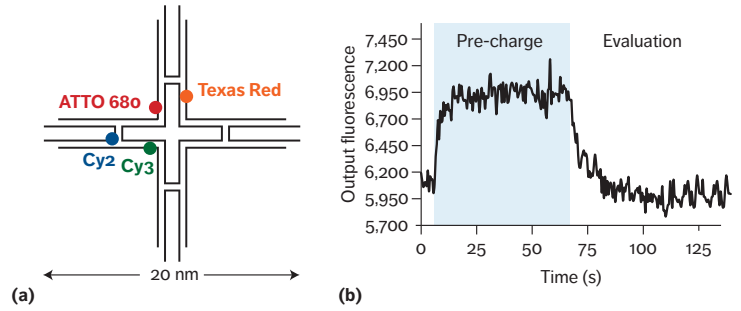

Figure 4. PASS gate experimental demonstration. (a) Fluorophore layout for the PASS gate on a DNA cross motif. Each black line represents a different DNA strand. (b) Output fluorescence from the PASS gate during both the pre-charge and evaluation phases when a logical 1 is applied to the input.

Validation of PCL Principles

Although dark states have been studied extensively under the context of stochastic super-resolution microscopy, very little has been done to engineer novel RET-based devices that take advantage of these states. So far, only a basic flip-flop and an optically tunable exciton router have been demonstrated.[13,16] To validate the operating principles of PCL, we expand on this body of evidence by providing an experimental demonstration of a working PASS gate and by simulating the PCL library in Figure 3.

Experimental Demonstration

We chose the PASS gate as a proof-of-concept device for its ability to demonstrate PCL principles with minimal design requirements.[17] To fabricate this device, we first selected suitable fluorophores for each terminal. Ultimately, we decided to use the commercially available fluorophores Cy2, Cy3, Texas Red, and ATTO 680 as the eval, mediator, output, and input fluorophores, respectively. Of these fluorophores, we found only ATTO 680 to be strongly susceptible to the dark state in the presence of MEA. Using a custom layout tool, we mapped the positions of these molecules to attachment sites on a DNA cross motif shown in Figure 4a based on the transfer efficiencies between fluorophores and the design principles discussed earlier. This nanostructure, which also could potentially host the other gates in Figure 3, measures roughly 20 nm on an edge, providing an estimate of the area required by individual

PCL gates. We then attached the fluorophores to their respective DNA strands and assembled the DNA motif according to a previously published protocol.[2] After fabrication, we added MEA to the sample and tested the device by exciting eval and monitoring the output fluorescence during both the pre-charge and evaluation phases. Although PCL operation requires eval to be illuminated only during evaluation, this experiment let us observe the output's rise and fall times, which ultimately dictate the minimum durations of each phase.

Figure 4b shows the output fluorescence from the PASS gate when a high input is applied. During the pre-charge phase, the input fluorophore is excited into its dark state, forcing the output fluorescence to rise. Although we used a 60-second pre-charge for this initial test, the duration of this phase can be drastically reduced, as the output signal saturates within approximately the first 10 seconds. As we described earlier, this rise time can be tuned based on the input excitation intensity.[10] During evaluation, the input excitation is removed. The output fluorescence begins high and is evaluated accordingly as a logical 1. As input fluorophores spontaneously return to their ground state, the output signal slowly decays back to its original 0 value. This phase should also be shortened, to approximately the first 5 seconds in this example, to ensure the output is correctly evaluated. The transition times for this proof-of-concept device are more than an order of magnitude shorter than those of typical DNA-based logic gates designed for similar computational domains.[4] Figure 4b shows only the case in which a high input is applied to the PASS gate. If instead a low input is applied, the input is not pre-charged into its dark state, and the output signal simply stays at its low fluorescence value throughout both the pre-charge and evaluation phases.

Continuous-Time Markov Chain Modeling

In addition to the experimental demonstration above, we modeled individual gates and cascades as CTMCs, which accurately describe the flow of excitons in RET systems.[18] Transfer efficiencies were set to conservative values achievable by real systems: 10 and 90 percent for low and high efficiencies, respectively. For the sake of simplicity, all fluorophores were assumed to have a lifetime of 3 ns and a quantum yield of 75 percent. Using these values in conjunction with Equation 1, which relates the transfer efficiency (TE) and the donor lifetime (τ_D) to the transfer rate (k_{RET}), we calculated the transition matrix for each CTMC.[7,18] We then numerically solved these models starting with an initially excited eval and monitoring the probability of output fluorescence. To test various input conditions, we set the transfer rates into and out of the dark fluorophores to zero and then determined the solution for the resulting CTMC.

$$k_{RET} = \frac{TE}{\tau_D(1 - TE)} \quad (1)$$

Individual gate results. Figure 5 summarizes the CTMC results by plotting the probability of output fluorescence, $P(F)$, for every input condition. For each gate, the probability of fluorescence from logical 1 outputs is much higher than logical 0 outputs, confirming that every gate performs the correct operation. Furthermore, the results clearly demonstrate the nonlinearity of PCL gates. The AND gate, for example, has a minimum on/off ratio of approximately 5.5 compared to the value of roughly 1.8 for its linear counterpart. This value can be improved even further using methods described in the following section.

Gates that rely only on inline inputs, such as NAND, NOR, and NPASS, exhibit infinite on/off ratios due to their complete removal of RET pathways when outputting a 0. When physically implemented, these on/off ratios will take on finite values determined either by undesirable RET pathways (such as direct transfer from eval to out) or simply by noise (for example, ambient light or the detector's dark current).

Gate optimizations. We can improve PCL gates that use mediator-input pairs, such as AND, OR, and PASS, by modifying the basic designs in Figure 3. The on/off ratios of these gates depend nonlinearly on the number of mediator-input pairs between eval and out. With each additional pair, the probability that an exciton makes it from eval to the output

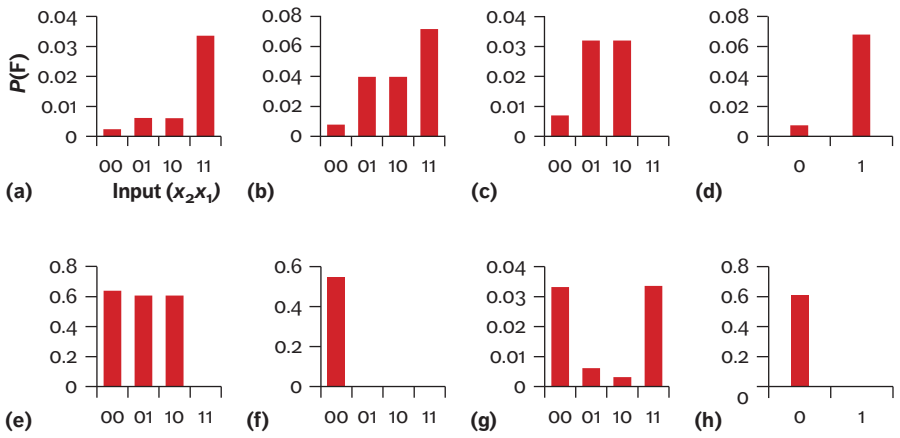

Figure 5. Output fluorescence probabilities for all input combinations of the (a) AND, (b) OR, (c) XOR, (d) PASS, (e) NAND, (f) NOR, (g) XNOR, and (h) NPASS PCL gates.

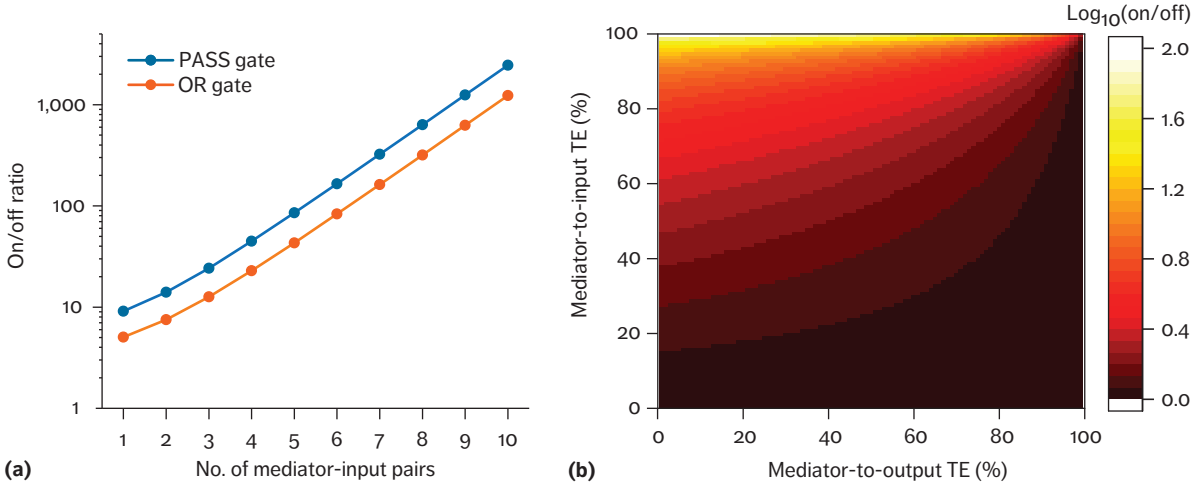

Figure 6. PCL gate performance improvements. (a) The on/off ratio for PASS and OR gates as a function of the number of mediator-input pairs. (b) The on/off ratio for a PASS gate with a single mediator-input pair as a function of both the mediator-to-input and mediator-to-output transfer efficiencies (TEs).

diminishes exponentially due to their serial layout. To demonstrate this concept, we varied the number of mediator-input pairs from 1 to 10 in both the PASS gate and in each parallel path of the OR gate. We then extracted the on/off ratio from each CTMC using the same efficiency, lifetime, and quantum yield parameters assumed earlier. The results in Figure 6a indicate that a PASS gate with just five additional mediator-input pairs exhibits an approximately 18-fold improvement over the basic one mediator-input design.

The on/off ratios of these devices also depend strongly on both the mediator-to-input and the mediator-to-output transfer efficiencies. Transfer from the mediator to the input should be as high as possible so that input fluorophores can efficiently steal excitons. Conversely, transfer from the mediator to the output, or any downstream fluorophore, should be kept as low as possible (while still providing observable output fluorescence) to avoid interfering with this exciton sinking process.

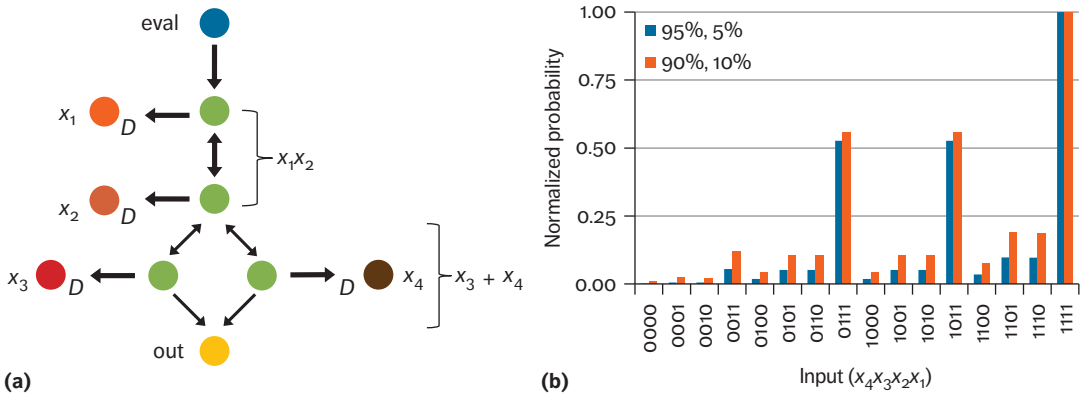

Figure 7. An example of a PCL cascade. (a) EFD for a PCL cascade representing $x_1x_2(x_3 + x_4)$. (b) Normalized output fluorescence probabilities from the cascade in (a) for all input conditions from two different models.

Figure 6b illustrates the effects of this design space on the on/off ratio for a PASS gate with only a single mediator-input pair. In this example, we set the eval-to-mediator transfer efficiency to 90 percent and varied the mediator-to-input and mediator-to-output efficiencies. Even with only a single mediator-input pair, the on/off ratio approaches 100 for designs with high mediator-to-input (99 percent) and low mediator-to-output (1 percent) efficiencies. This is more than an order of magnitude greater than the basic design proposed.

PCL cascades. PCL gates can also be cascaded to create more complex circuits. Cascades are formed by connecting multiple inputs to a single mediator path from eval to out. All inputs are applied simultaneously during the precharge phase, and the evaluation phase follows as normal. By using the same mediator fluorophore throughout the circuit, the spectral content of a PCL cascade scales only with the number of inputs.

Figure 7a shows the EFD for an AND-OR cascade performing the logical operation out $= x_1x_2(x_3 + x_4)$. We modeled this EFD using two sets of high and low transfer efficiencies: 90 percent and 10 percent (90/10) and 95 percent and 5 percent (95/5). Figure 7b plots the normalized output fluorescence probabilities from each model. Both function as designed, with input conditions 0111 ($x_4x_3x_2x_1$), 1011, and 1111 resulting in significantly more fluorescence than all other input conditions. The 95/5 model outperforms the 90/10 model by offering lower relative logical 0 outputs for the reasons we described in the previous section. Although we illustrated only a serial cascade, which implements the products of logic gates, parallel cascades implementing the sums of logic gates are also possible using multiple mediator paths that converge to a single output. Note that cascades can also contain gates with inline inputs; however, the mediator chain must undergo an additional red-shift after these inputs. It should even be possible to use the output from one cascade to act as the input to another, enabling the implementation of more complex circuits. Given this large design space, we leave a full exploration of PCL cascades, including analyses of multi-eval and multi-output circuits along with their associated limitations, as future work.

We presented a new RET logic design methodology that harnesses the dark states of fluorescent molecules to produce a set of nonlinear logic gates. Preliminary experimental evidence suggests that these design principles are sound. Furthermore, CTMC modeling of each gate has illustrated that individual gates produce the correct operations and that there are realistic design parameters for improving the performance

of these devices. Although gate-level experimental characterization is necessary before larger circuits are fabricated, this work shows that RET logic has the potential to build complex integrated systems at unprecedented scales for use in new computational domains.

Acknowledgments

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