On-chip Parallelism

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CPS 220

Administivia

- Homework #5 Due Today
- Homework #6 Due Dec 6

Projects
- Presentations Dec 6 (or Dec 4 & Dec 6)
- Documents ~10 pages
  - Good writing is important
  - Progress is important
- Final is Dec 14

Multithreaded Processors

- Exploit thread-level parallelism to improve performance
  - Multiple Program Counters
- Thread
  - Independent programs (multiprogramming)
  - Threads from same program

Deneclor HEP

- General purpose scientific computer
- Organized as MP
  - Up to 16 processors
  - Each processor multithreaded
  - Up to 128 memory modules
  - Up to 4 I/O cache modules
  - Three-input switches and chaotic routing

HEP Processor Organization

- Multiple contexts (threads)
  - Each has own Program Status Word (PSW)
- PSWs circulate in control loop
  - Control and data loops pipelined 8 deep
  - PSW in control can circulate no faster than data in data loop
  - PSW at queue head fetches and starts execution of next instruction
- Clock period: 100ns
  - 8 PSWs in control loop ⇒ 10MIPS
  - Each thread gets 1/8 the processor
  - Maximum performance per thread ⇒ 1.25 MIPS
  - (And they tried to sell as supercomputer)

Simultaneous Multithreading

- Goal: use hardware resources more efficiently
  - Especially for superscalar processors
- Assume 4-issue superscalar
- Alpha 21464

Thread Instruction

Horizontal Waste

Vertical Waste
Operation of Simultaneous Multithreading

- Standard multithreading can reduce vertical waste
- Issue from multiple threads in same clock cycle
- Eliminate both horizontal and vertical waste
- Larger Register Files

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Limitations of SuperScalar Architectures

Instruction Fetch
- Branch prediction
- Alignment of packet of instructions

Dynamic Instruction Issue
- Need to identify ready instructions
- Rename Table
  - No compares
  - Large number of ports (Operands x Width)
- Issue Queue Size
  - \( n \times O \times W \) 1 bit comparators (src and dest)
  - Quadratic increase in queue size with issue width
  - PA-8000 20% of die area to issue queue (56 instruction window)

SuperScalar Limitations (Continued)

Instruction Execute
- Register File
  - More rename registers
  - More access ports
  - Complexity quadratic with issue width
- Bypass logic
  - Complexity quadratic with issue width
  - Wire delays
- Functional Units
  - Replicate
  - Add ports to data cache (complexity adds to access time)

Why Single Chip MP?

- Technology Push
  - Benefits of wide issue are limited
  - Decentralized microarchitecture: easier to build several simple fast processors than one complex processor
- Application Pull
  - Applications exhibit parallelism at different grains
  - < 10 instructions per cycle (Integer codes)
  - > 40 instructions per cycle (FP loops)

A 6-Way SuperScalar Processor

A 4 x 2 Single Chip Multiprocessor
Performance Comparison

Summary of Performance

- 4 x 2 MP works well for coarse grain apps
  - How well would Message Passing Architecture do?
  - Can SUIF handle pointer intensive codes?
- For “tough” codes 6-way does slightly better, but neither is > 60% better than 2-issue