Department of Computer Science
Duke University
Ph.D. Qualifying Exam

ID: _____

Computer Architecture
180 minutes

Not all questions are equally difficult. Look at entire exam. Budget time carefully. Please carefully state any assumptions you make.
Please write your name on every page in the exam.

Reading Academic Policy:	5 pts
Question 1	20pts
Question 2	20pts
Question 3	15pts
Question 4	10pts
Question 5	15pts
Question 6	15pts

Academic Policy: University policy will be strictly enforced. Zero tolerance for cheating or plagiarism. If a student is suspected of academic dishonesty, faculty are required to report the matter to the Office of Student Conduct. A student found responsible for academic dishonesty faces formal disciplinary actions, which may include suspension. A student suspended twice for academic dishonesty automatically faces a minimum 5-year separation from Duke University.

I have read and understood the academic policy. Check the appropriate entry below.

_____(Yes) _____(No)

Question 1. Caches [20]

Mark whether the following modifications to the cache cause each of the 3C's to change. Assume the baseline cache is set-associative. Explain your reasoning to receive full credit.

1A – Increase number of ways (i.e., associativity) (5pts)

Compulsory Misses:	increase	decrease	no effect
Conflict Misses:	increase	decrease	no effect
Capacity Misses:	increase	decrease	no effect

1B – Increase number of bytes per cache line (i.e., cache block) (5pts)

Compulsory Misses:	increase	decrease	no effect
Conflict Misses:	increase	decrease	no effect
Capacity Misses:	increase	decrease	no effect

1C – Calculating Cache Parameters (5pts)

Suppose a cache is addressed with 32 bits. This address is partitioned in index, tag, and offset. The index is 8 bits and the offset is 4 bits. Calculate the following cache parameters for a two-way set associative cache.

Tag Size (bits) =

Cache Line Size (bytes) =

Number of Sets =

Cache Capacity (kilobytes) =

1D – Virtual Memory (5pts)

What is the role of the translation lookaside buffer (TLB)?

Question 2. Processor Performance [20]

(Instructions / Program) x (Cycles / Instruction) x (Seconds / Cycle) = Seconds / Program

Circle whether the following modifications will cause each category to increase, decrease, or have no effect. These modifications are made to a standard out-of-order, superscalar processor with register renaming and branch prediction. For each modification, assume the rest of the machine remains unchanged. Explain you reasoning to receive full credit.

2A – Perform loop unrolling (10pts)

Instructions / Program:	increase	decrease	no effect
Cycles / Instruction:	increase	decrease	no effect
Seconds / Cycle:	increase	decrease	no effect

2B – Switch from a datapath with no forwarding to complete forwarding (a.k.a. bypassing) (10pts)

Instructions / Program:	increase	decrease	no effect
Cycles / Instruction:	increase	decrease	no effect
Seconds / Cycle:	increase	decrease	no effect

Question 3. Processor Microarchitecture [15]

3A (10pts)

Out-of-order processors can execute loads and stores speculatively, but must check for dependences between them. Describe (i) how to identify dependences and (ii) what speculative load instructions must do when there are store instructions in progress (i.e., not yet committed).

3B (5pts)

What purpose does the reorder buffer serve in an out-of-order processor?

Question 4. Instruction-Level Parallelism [10]

4A (5pts)

Show a MIPS instruction sequence that would cause a data hazard in a five-stage pipeline.

4B (5pts)

Fill in the blanks by choosing the correct word from the two choices.

Pipelining is a performance optimization that takes a datapath and reduces the clock (i) _____, increases the clock (ii) _____, and (iii) increases instruction (iii) _____.

(i) _____ (frequency or period)

(ii) _____ (frequency or period)

(iii) _____ (latency or throughput)

Question 5. Coherence and Consistency [15]

5A (10pts)

Suppose a processor reads a memory location X that is dirty in another processor's cache. The directory will observe this read request. Suppose a three-state invalidate protocol is used. What action must the remote processor perform? How does the directory support this action?

5B (5pts)

Define sequential consistency. Provide Lamport's definition. Alternatively, specify the conditions on loads/stores that that must hold in a sequentially consistent machine.

Question 6. Assorted Questions [15]

6A (5pts)

What is Amdahl's Law? Write down the equation and explain in words why computer architects care about it.

6B (5pts)

The computer architect has two options for reducing power. First, reduce clock frequency from 4GHz to 2GHz. Second, decrease voltage from 1.2 to 1.0V. How much power is saved in each strategy?

6C (5pts)

Pipelining was a popular technique for improving performance in the late 1990s. But it encountered higher overheads and diminishing returns in performance. What is the source of overheads when a processor datapath is broken into more and more pipeline stages?