Department of Computer Science
Duke University
Ph.D. Qualifying Exam, Fall 2018

Name:_____

Computer Architecture
180 minutes

Not all questions are equally difficult. Look at entire exam. Budget time carefully.
Please carefully state any assumptions you make.
Please write your name on every page in the exam.

Signing Academic Policy:	5 pts
Question 1	20pts
Question 2	25pts
Question 3	20pts
Question 4	20pts
Question 5	20pts

Academic Policy: University policy will be strictly enforced. Zero tolerance for cheating or plagiarism. If a student is suspected of academic dishonesty, faculty are required to report the matter to the Office of Student Conduct. A student found responsible for academic dishonesty faces formal disciplinary actions, which may include suspension. A student suspended twice for academic dishonesty automatically faces a minimum 5-year separation from Duke University.

I have read and understood the academic policy.

_____ (signature)

[20 points] Question 1. Caches

[8 points] a) Suppose a cache is addressed with 32 bits. This address is partitioned in index, tag, and offset. The index is 9 bits and the offset is 5 bits. Calculate the following cache parameters for a four-way set associative cache.

Tag Size (bits) =

Cache Line Size (bytes) =

Number of Sets =

Cache Capacity (kilobytes) =

[6] b) Why do modern virtual memory systems use a tree instead of a vector (or list or table) to represent the page table?

[6] c) Does a TLB miss always cause a page fault? Explain why or why not?

[25 points] Question 2: High-performance processor cores

[5] a) Write a snippet of assembly code (no more than 5 instructions) with a lot of ILP. Assume register renaming. Please comment the code if it's not MIPS assembly.

[5] b) Write a snippet of code (no more than 5 instructions) with little ILP. Assume register renaming. Please comment the code if it's not MIPS assembly.

[5] c) Write a snippet of 3 instructions and show how they'd be renamed by a modern core. Show the rename table at each step. Please comment the code if it's not MIPS assembly.

[10] d) In an ideal world, a 1-wide core pipeline with N stages would achieve an improvement in throughput of N compared to a 1-wide unpipelined core. Why does a real pipelined core with N stages not achieve that throughput? Please provide two distinct reasons.

[20 points] Question 3: Static scheduling of instructions

[10] a) What is the purpose of loop unrolling? Show a short example.

[10] b) What is the purpose of instruction predication? Show a short example.

[20 points] Question 4: Branches and Speculation

[10] a) Why are more branches taken than not taken?

[10] b) What happens to the reorder buffer when a branch is determined to have been mispredicted?

[20 points] Question 5: Coherence and Consistency

[10] a) Intel and AMD processors adhere to the Total Store Order (TSO) memory consistency model. Describe TSO's constraints on the orderings of loads and stores.

[10] b) Many cache coherence protocols use a subset of the MOESI coherence states to denote the state of a block in a cache. Please explain what the M, S, and I states stand for and what they mean in terms of the cache's ability to read and write a block in each of those states.